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CHI MEI OPTOELECTRONICS CORP.

Issued Date: Jun. 13, 2005
Model No.: N154I1-L0A
Approval

TFT LCD Approval Specification

MODEL NO.: N154I1-L0A

Customer : _____

Approved by : _____

Note :

Liquid Crystal Display Division	
QRA Division.	OA Head Division.
Approval	Approval
陳 94. 6. 13 永一	林 94. 6. 13 添仁

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 0.0	Jan. 18,'05	All	All	Tentative specification first issued.
Ver 1.0	Jan. 20,'05	All	All	Preliminary specification first issued.
Ver 1.1	Feb. 14,'05	14-16	5.5	Modify the EDID code for IBM request.
Ver 2.0	Jun. 13,'05	All	All	Approval specification first issued.

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

N154I1 -L0A is a 15.4" TFT Liquid Crystal Display module with single CCFL Backlight unit and 30 pins LVDS interface. This module supports 1280 x 800 Wide-XGA mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The inverter module for Backlight is not built in.

1.2 FEATURES

- Thin and light weight
- WXGA (1280 x 800 pixels) resolution
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 1 pixel/clock
- DE only mode

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	331.2 (H) x 207.0 (V) (15.4" diagonal)	mm	(1)
Bezel Opening Area	335.0 (H) x 210.7 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1280 x R.G.B. x 800	pixel	-
Pixel Pitch	0.2588 (H) x 0.2588 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), AG Type	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	343.5	344.0	344.5	mm	(1)
	Vertical(V)	221.5	222.0	222.5	mm	
	Depth(D)	-	6.2	6.5	mm	
Weight		-	600	620	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

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2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

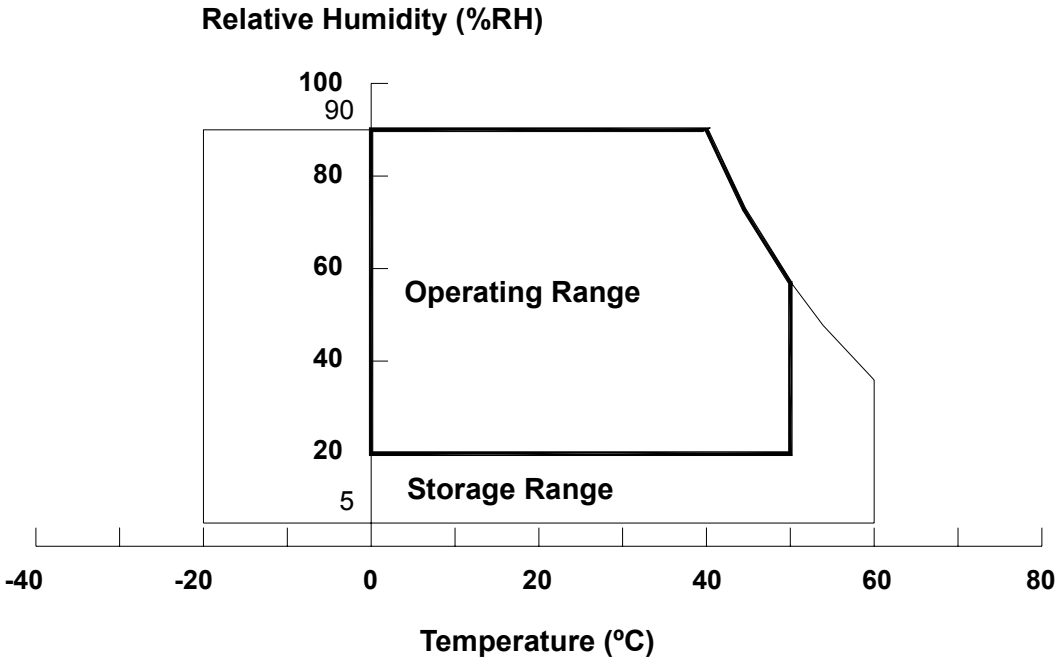
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	220	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

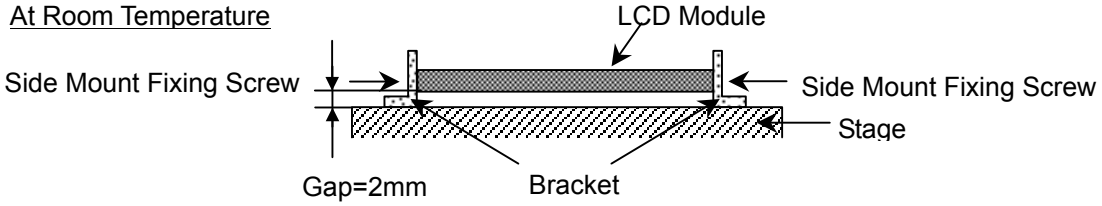
(c) No condensation .



Note (2) The temperature of panel surface should be 0 ºC Min. and 50 ºC Max.

Note (3) 2ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 0.5 Hr / Cycle, 1 cycles for each X, Y, Z. The fixing condition is shown as below:



Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

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2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	Vcc+0.3	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_L	-	2.5K	V_{RMS}	(1), (2), I_L = 6.5 mA
Lamp Current	I_L	-	7.0	mA_{RMS}	(1), (2)
Lamp Frequency	F_L	-	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to Section 3.2 for further information).

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3. ELECTRICAL CHARACTERISTICS

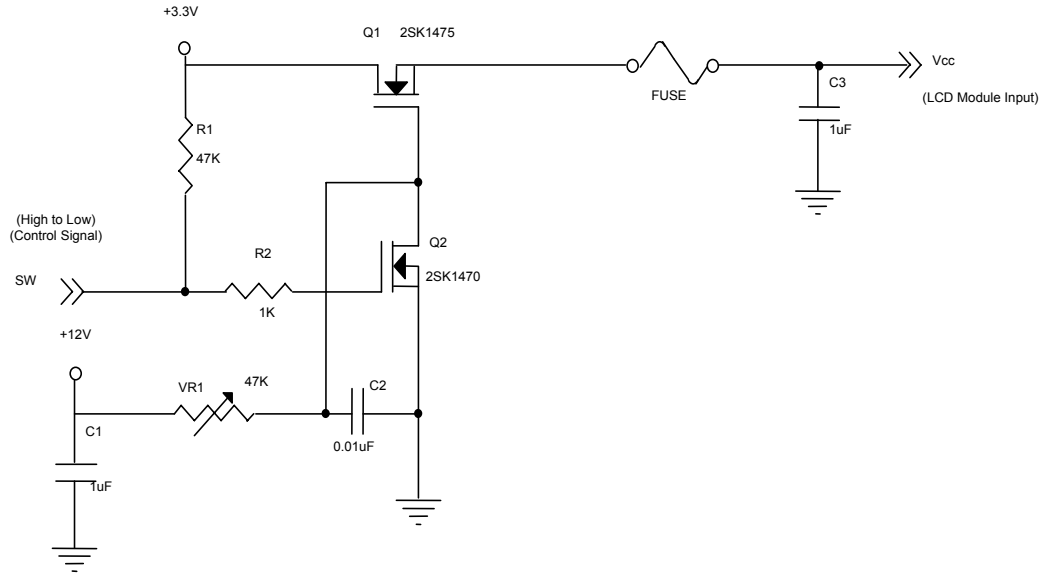
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

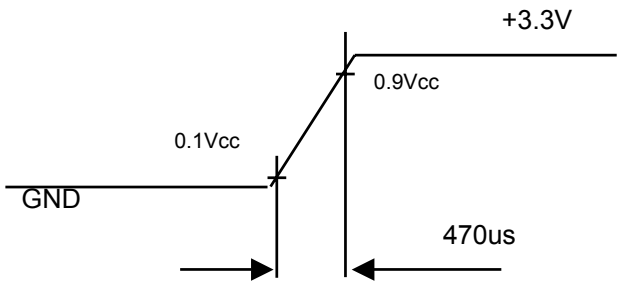
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	3.0	3.3	3.6	V	-
Ripple Voltage		V_{RP}	-	-	100	mV	-
Rush Current		I_{RUSH}	-	-	1.5	A	(2)
Power Supply Current	White	Icc	-	400		mA	(3)a
	Black		-	520		mA	(3)b
	Vertical Stripe		-	560		mA	(3)c
Differential Input Voltage for LVDS Receiver Threshold	"H" Level	V_{IH}	-	-	+100	mV	-
	"L" Level	V_{IL}	-100	-	-	mV	-
Terminating Resistor		R_T	-	100	-	Ohm	-

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



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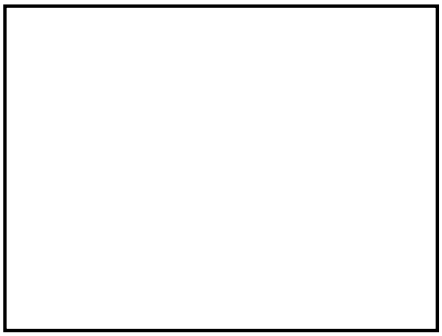
Note (3) The specified power supply current is under the conditions at Vcc = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

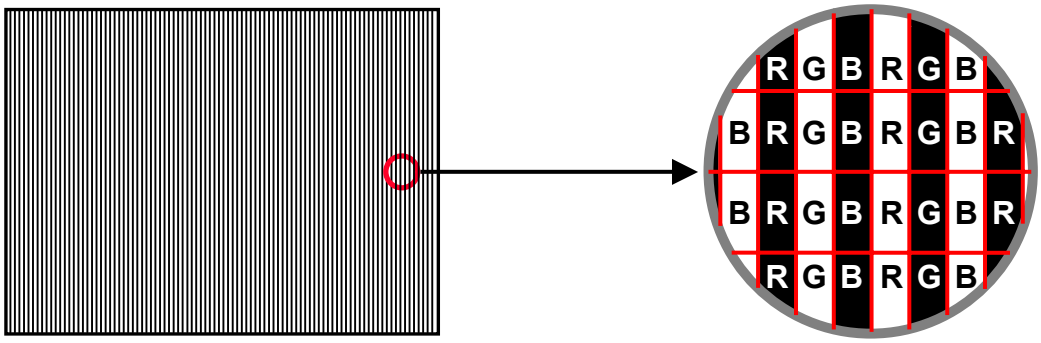


Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



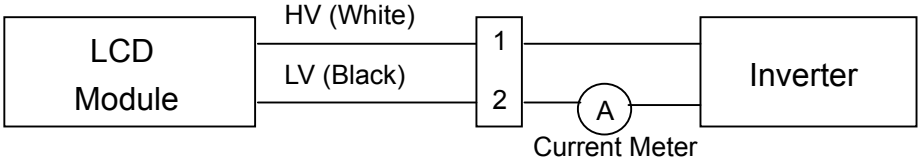
Active Area

3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	612	680	748	V_{RMS}	I_L = 6.5 mA
Lamp Current	I_L	2.0	6.0	6.5	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	-	1110, 25℃	V_{RMS}	(2)
		-	-	1300, 0℃	V_{RMS}	(2)
Operating Frequency	F_L	50	-	80	KHz	(3)
Lamp Life Time	L_{BL}	10,000	-	-	Hrs	(5)
Power Consumption	P_L	-	4.08	-	W	(4), I_L = 6.5 mA

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

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Note (3) The lamp frequency may generate interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L$

Note (5) The lifetime of lamp is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and I_L = 6.5 mA_{RMS} until one of the following events occurs:

(a) When the brightness becomes ≦ 50% of its original value.

(b) When the effective ignition length becomes ≦ 80% of its original value. (Effective ignition length is defined as an area that the brightness is less than 70% compared to the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid generating too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

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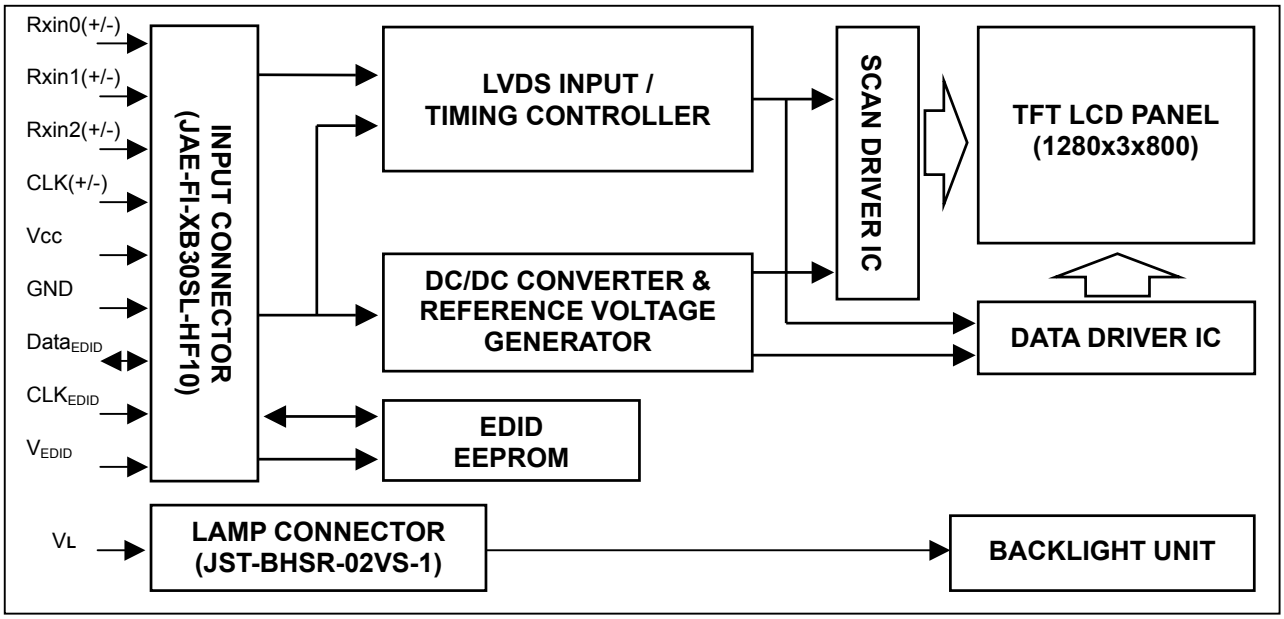
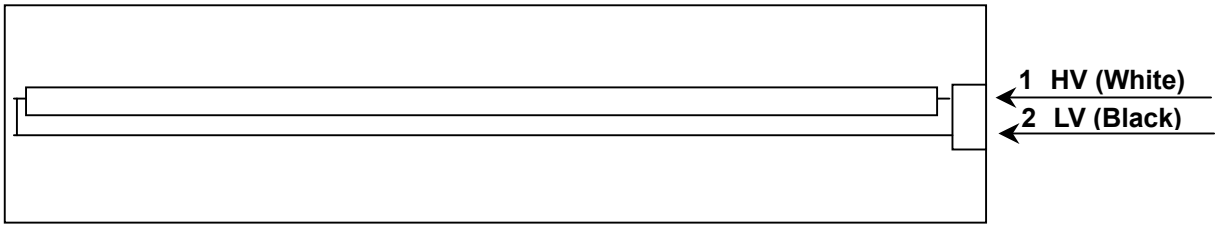
4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



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5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		-
2	Vcc	Power Supply +3.3 V		-
3	Vcc	Power Supply +3.3 V		-
4	V_{EDID}	DDC +3.3 V		
5	NC	-	-	-
6	CLK_{EDID}	DDC Clock		
7	$Data_{EDID}$	DDC Data		
8	Rxin0-	LVDS Differential Data Input	Negative	-
9	Rxin0+	LVDS Differential Data Input	Positive	R0~R5,G0
10	Vss	Ground		
11	Rxin1-	LVDS Differential Data Input	Negative	-
12	Rxin1+	LVDS Differential Data Input	Positive	G1~G5,B0,B1
13	Vss	Ground		
14	Rxin2-	LVDS Differential Data Input	Negative	-
15	Rxin2+	LVDS Differential Data Input	Positive	B2~B5,Hsync,Vsync,DE
16	Vss	Ground		
17	CLK-	LVDS Clock Data Input	Negative	
18	CLK+	LVDS Clock Data Input	Positive	LVDS Level
19	Vss	Ground		
20	NC	-	-	-
21	NC	-	-	-
22	NC	-	-	-
23	NC	-	-	-
24	NC	-	-	-
25	NC	-	-	-
26	NC	-	-	-
27	NC	-	-	-
28	NC	-	-	-
29	NC	-	-	-
30	NC	-	-	-

Note (1) Connector Part No.: JAE-FI-XB30SL-HF10 or equivalent

Note (2) User's connector Part No: JAE-FI-X30C2L or equivalent

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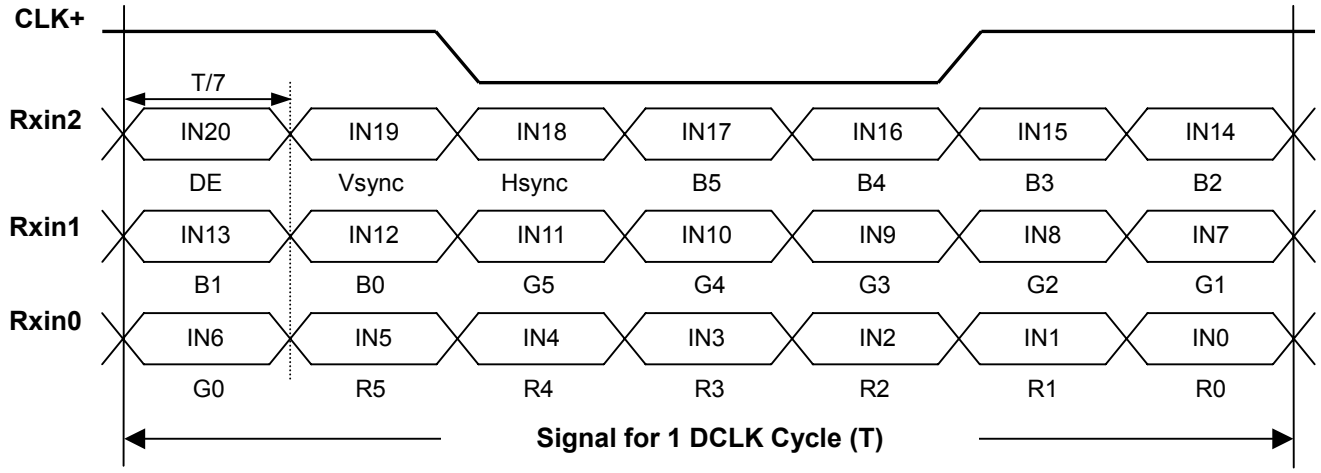
5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	White
2	LV	Ground	Black

Note (1) Connector Part No.: JST-BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: JST-SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL



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5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header , Fixed	00	00000000
1	1	Header , Fixed	FF	11111111
2	2	Header , Fixed	FF	11111111
3	3	Header , Fixed	FF	11111111
4	4	Header , Fixed	FF	11111111
5	5	Header , Fixed	FF	11111111
6	6	Header , Fixed	FF	11111111
7	7	Header , Fixed	00	00000000
8	8	ID system Manufacturer Name	24	00100100
9	9	Compressed ASCII	4D	01001101
10	0A	ID Product Code	74	01110100
11	0B	ID Product Code	23	00100011
12	0C	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
13	0D	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
14	0E	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
15	0F	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
16	10	Week of manufacture 1 - 53 (unused: 00h) : 00h fixed by CMO	00	00000000
17	11	Year of manufacture year - 1990(unsed:00h) : 00h fixed by CMO	00	00000000
18	12	Version=1	01	00000001
19	13	Revision=3	03	00000011
20	14	Digital	80	10000000
21	15	Active area horizontal 33.12cm	21	00100001
22	16	Active area vertical 20.70cm	15	00010101
23	17	gamma * 100-100 = 2.2*100-100=120	78	01111000
24	18	Feature support (no DPMS, Active off, RGB, Preferred Timing Mode)	0A	00001010
25	19	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0	63	01100011
26	1A	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0	45	01000101
27	1B	Rx=0.603	9A	10011010
28	1C	Ry=0.334	55	01010101
29	1D	Gx=0.316	51	01010001
30	1E	Gy=0.538	89	10001001
31	1F	Bx=0.157	28	00101000
32	20	By=0.137	23	00100011
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Not supported	00	00000000
36	24	Not supported	00	00000000
37	25	No manufacturer's specific timing	00	00000000
Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001

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40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock (“71.11MHz”, According to VESA CVT Rev1.1)	C7	11000111
55	37	71.11MHz/10000 = 7111 = 1BC7h(hex LSB first)	1B	00011011
56	38	HActive(D7-D0) = 1280 mod 256	00	00000000
57	39	HBlank(D7-D0) = 160 mod 256	A0	10100000
58	3A	HActive(D11-D8) : HBlank(D11-D8) = 1280/256 : 160/256	50	01010000
59	3B	VActive(D7-D0) = 800 mod 256	20	00100000
60	3C	VBlank(D7-D0) = 23 mod 256	17	00010111
61	3D	VActive(D11-D8) : VBlank(D11-D8) = 800/256 : 23/256	30	00110000
62	3E	HSyncOffset(D7-D0) = HBorder+HFrontPorch = 48	30	00110000
63	3F	HSyncWidth(D7-D0) = 32	20	00100000
64	40	VSyncOffset(D3-D0) : VSyncWidth(D3-D0)	36	00110110
65	41	HSyncOffset(D9-D8) : HSyncWidth(D9-D8) : VSyncOffset(D5-D4) : VSyncWidth(D5-D4)	00	00000000
66	42	HImageSize(mm, D7-D0) = 331 mod 256	4B	01001011
67	43	VImageSize(mm, D7-D0) = 207 mod 256	CF	11001111
68	44	HImageSize(D11-D8) : VImageSize(D11-D8) = 331/256 : 207/256	10	00010000
69	45	Hborder=0	00	00000000
70	46	Vborder=0	00	00000000
71	47	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1C	00011100
72	48	Pixel Clock/10,000 (LSB)	26	00100110
73	49	Pixel Clock/10,000 (MSB) /	17	00010111
74	4A	HActive(D7-D0) = 1280 mod 256	00	00000000
75	4B	HBlank(D7-D0) = 160 mod 256	A0	10100000
76	4C	HActive(D11-D8) : HBlank(D11-D8) = 1280/256 : 160/256	50	01010000
77	4D	VActive(D7-D0) = 800 mod 256	20	00100000
78	4E	VBlank(D7-D0) = 23 mod 256	17	00010111
79	4F	VActive(D11-D8) : VBlank(D11-D8) = 800/256 : 23/256	30	00110000
80	50	HSyncOffset(D7-D0) = HBorder+HFrontPorch = 48	30	00110000
81	51	HSyncWidth(D7-D0) = 32	20	00100000
Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
82	52	VSyncOffset(D3-D0) : VSyncWidth(D3-D0)	36	00110110

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83	53	HSyncOffset(D9-D8) : HSyncWidth(D9-D8) : VSyncOffset(D5-D4) : VSyncWidth(D5-D4)	00	00000000
84	54	HImageSize(mm, D7-D0) = 331 mod 256	4B	01001011
85	55	VImageSize(mm, D7-D0) = 207 mod 256	CF	11001111
86	56	HImageSize(D11-D8) : VImageSize(D11-D8) = 331/256 : 207/256	10	00010000
87	57	Hborder=0	00	00000000
88	58	Vborder=0	00	00000000
89	59	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1C	00011100
90	5A	Flag	00	00000000
91	5B	Flag	00	00000000
92	5C	Flag	00	00000000
93	5D	Data type tag : 0Fh	0F	00001111
94	5E	Flag	00	00000000
95	5F	Low **Refresh Rate #1** (Horizontal active pixels / 8) - 31=129(81h)	81	10000001
96	60	Low **Refresh Rate #1** Image Aspect ratio(16 : 10)	0A	00001010
97	61	Low **Refresh Rate #1** Refresh Rate=50Hz	32	00110010
98	62	Low **Refresh Rate #2** (Horizontal active pixels / 8) - 31=129(81h)	81	10000001
99	63	Low **Refresh Rate #2** Image Aspect ratio(16 : 10)	0A	00001010
100	64	Low **Refresh Rate #2** Refresh Rate=40Hz	28	00101000
101	65	Brightness (1/10nit) , 300/10=30(1Eh)	1E	00011110
102	66	Feature Flags	01	00000001
103	67	Reserved	00	00000000
104	68	EISA manufacturer code(3 Character ID) -CMO	0D	00001101
105	69	Compressed ASCII	AF	10101111
106	6A	Panel Supplier Reserved - Product code -1509	09	00001001
107	6B	(Hex, LSB first)	15	00010101
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data type tag : FEh	FE	11111110
112	70	Flag	00	00000000
113	71	"N"	4E	01001110
114	72	"1"	31	00110001
115	73	"5"	35	00110101
116	74	"4"	34	00110100
117	75	"I"	49	01001001
118	76	"1"	31	00110001
119	77	Terminator: 0Ah	0A	00001010
120	78	padding: 20h	20	00100000
121	79	padding: 20h	20	00100000
122	7A	padding: 20h	20	00100000
123	7B	padding: 20h	20	00100000
124	7C	padding: 20h	20	00100000
125	7D	padding: 20h	20	00100000
126	7E	No extension	00	00000000
127	7F	One-byte checksum of entire 128 bytes EDID equals 00h.	4B	01001011

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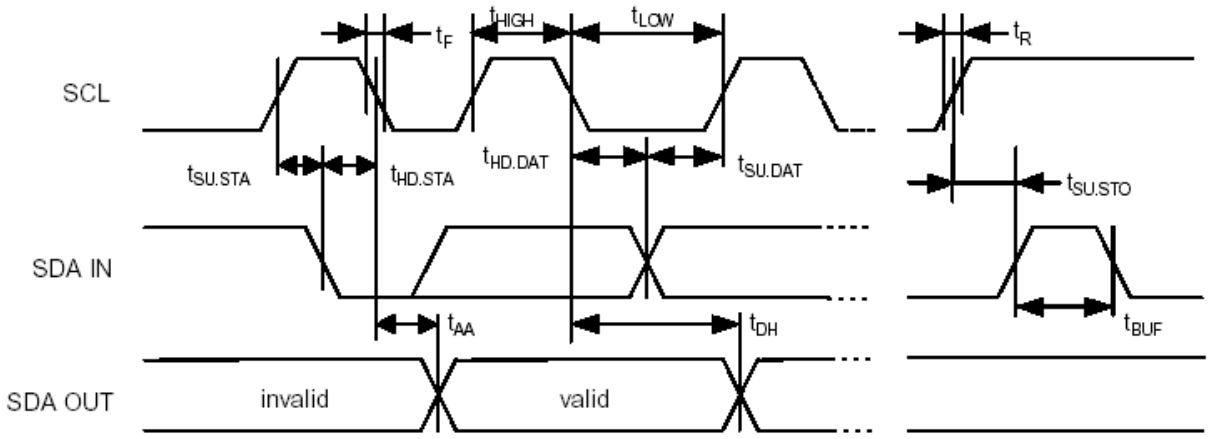
5.6 EDID SIGINAL SPECIFICATION

(1) EDID Power

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	—	2.7	—	5.5	V



(2) DC characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current Vcc=5.0V	Icc	READ at 100kHz	—	0.4	1.0	mA
Supply current Vcc=5.0V	Icc	WRITE at 100kHz	—	2.0	3.0	mA
Standby Current	ISB	Vin=Vcc or Vss	—	1.6	4.0	μA
Input Leakage Current	ILI	Vin=Vcc or Vss	—	0.1	3.0	μA
Onput Leakage Current	ILO	Vout=Vcc or Vss	—	0.05	3.0	μA
Input Low Level	VIL	—	-1.0	—	Vcc x 0.3	V
Input High Level	VIH	—	Vcc x 0.7	—	Vcc+0.5	V
Output Low Level Vcc=1.8V	VOL1	IOL=0.15mA	—	—	0.2	V

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Output Low Level Vcc=3.0V	VOL2	IOL=2.1mA	—	—	0.4	V

(3) AC characteristics (VCC=2.5~5.5V standard operation mode)

Parameter	Symbol	Min	Max	Unit
Clock Frequency, SCL	FSCL	—	100	kHz
Clock Pulse Width Low	TLOW	4.7	—	μs
Clock Pulse Width High	THIGH	4.0	—	μs
Noise Suppression Time	TI	—	100	ns
Clock Low to Data Out Valid	TAA	0.1	4.5	μs
Time the bus must be free before a new transmission can start	TBUF	4.7	—	μs
Start Hold Time	THD.STA	4.0	—	μs
Start Set-up Time	TSU.STA	4.7	—	μs
Data in Hold Time	THD.DAT	0	—	μs
Data in Set-up Time	TSU.DAT	200	—	ns
Inputs Rise Time	TR	—	1.0	μs
Inputs Fall Time	TF	—	300	ns
Stop Set-up Time	TSU.STO	4.7	—	μs
Data Out Hold Time	TDH	100	—	ns
Write Cycle Time	TWR	—	10	ms

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6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

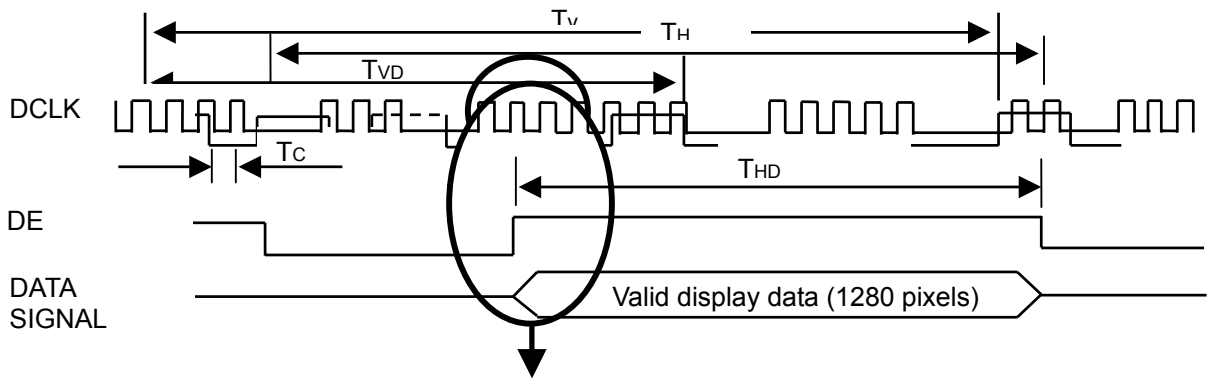
The input signal timing specifications are shown as the following table and timing diagram.

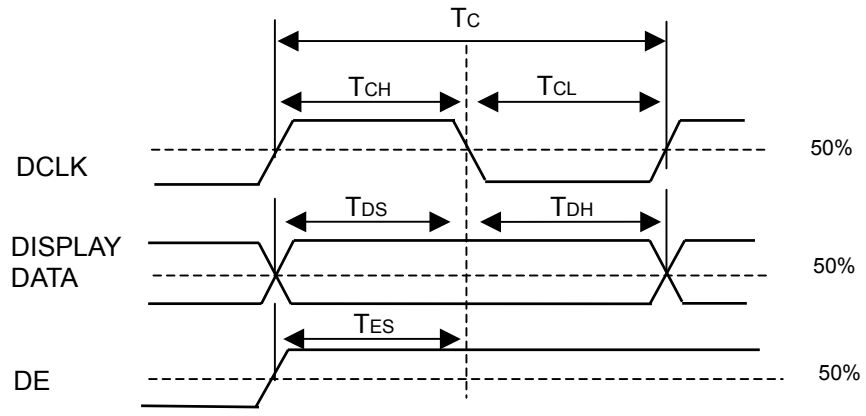
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Clock	Frequency	1/Tc	-	71	80	MHz	-
	High Time	T_{CH}	13	-	-	nsec	-
	Low Time	T_{CL}	13	-	-	nsec	-
Data	Setup Time	T_{DS}	4	-	-	nsec	-
	Hold Time	T_{DH}	4	-	-	nsec	-
Vsync Frequency	Frequency	Vsync	-	60	-	Hz	
Hsync Frequency	Frequency	Hsync	-	49.4	-	KHz	
Data Enable	Pulse width	T_{DEP}	100	-	-	clocks	(1)
Data Enable	Setup Time	T_{ES}	3.5	4.0	-	nsec	(1)
Frame Frequency	Cycle	T_V	804	823	2000	lines	-
Vertical Active Display Term	Display Period	T_{VD}	800	800	800	lines	-
One Line Scanning Time	Cycle	T_H	1350	1440	2000	clocks	(2)
Horizontal Active Display Term	Display Period	T_{HD}	1280	1280	1280	clocks	-

Note (1) Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

Note (2) The duration of DE signal must be longer than 1 clock period at every horizontal sync. period.

INPUT SIGNAL TIMING DIAGRAM





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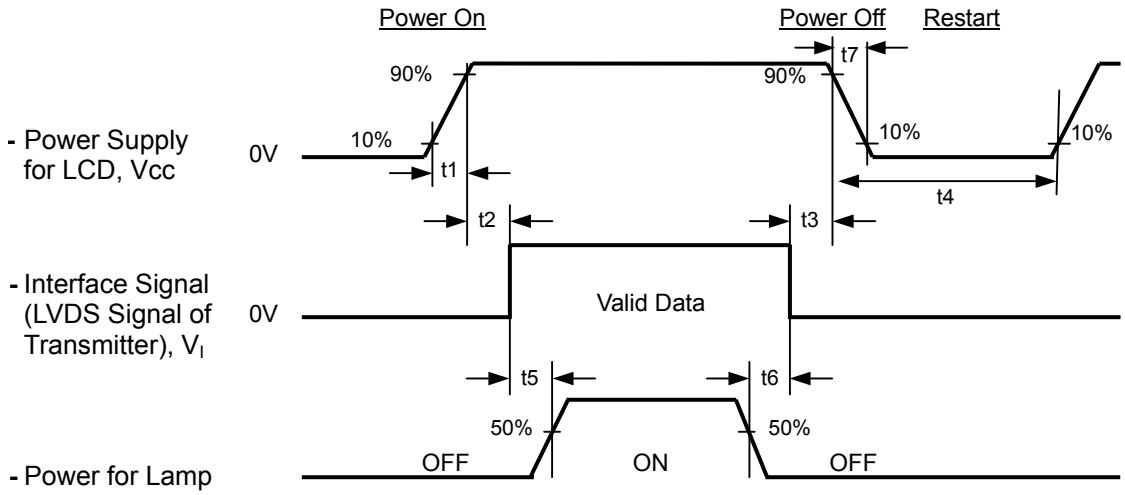
6.2 POWER ON/OFF SEQUENCE



Timing Specifications:

0.5 <t1 ≦ 10 msec

0 < t2 ≦ 50 msec

0 < t3 ≦ 50 msec

t4 ≧ 150 msec

t5 ≧ 200 msec

t6 ≧ 200 msec

Note (1) Please avoid floating state of interface signal at invalid period.

Note (2) When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time had better to follow

t7 ≧ 5 msec

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7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I_L	(6.5)	mA
Inverter Driving Frequency	F_L	(55)	KHz
Inverter	Sumida-H05-4915		

The measurement methods of optical characteristics are shown in Section 7.2. The following items should be measured under the test conditions described in Section 7.1 and stable environment shown in Note (6).

7.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	385	550	-	-	(2), (5)
Response Time		T_R		-	4	9	ms	(3)
		T_F		-	16	21	ms	
Average Luminance of White		L_{AVE}		260	300	-	cd/m^2	(5), (6)
White Variation		δW		-	-	1.4	-	(5), (6)
Cross Talk		CT		385	550	-	%	(4), (5)
Color Chromaticity	Red	Rx		0.563	0.593	0.623	(1), (5)	(1), (6)
		Ry		0.309	0.339	0.369		
	Green	Gx		0.289	0.319	0.349		
		Gy		0.500	0.530	0.560		
	Blue	Bx		0.120	0.150	0.180		
		By		0.101	0.131	0.161		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
Viewing Angle	Horizontal	θ_x+	CR≥10	50	60	-	(1), (5)	(1), (6)
		θ_x-		50	60	-		
	Vertical	θ_Y+		30	40	-		
		θ_Y-		50	60	-		

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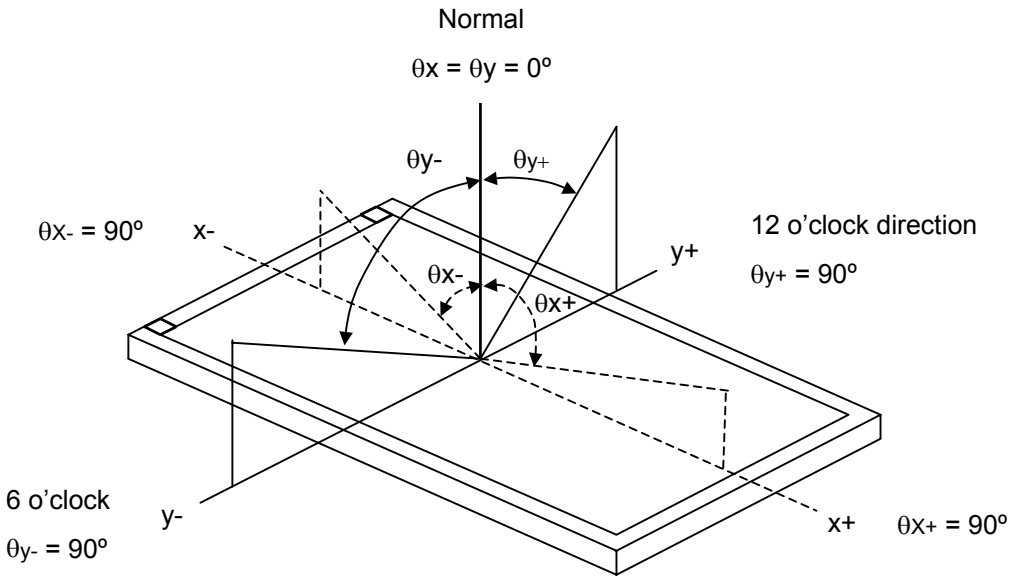
Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

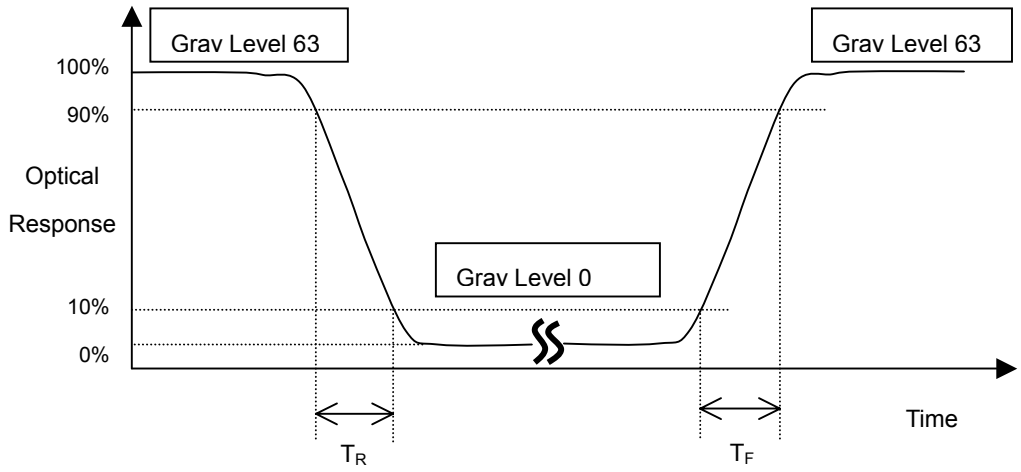
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



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Note (4) Definition of Average Luminance of White (L_{AVE}):

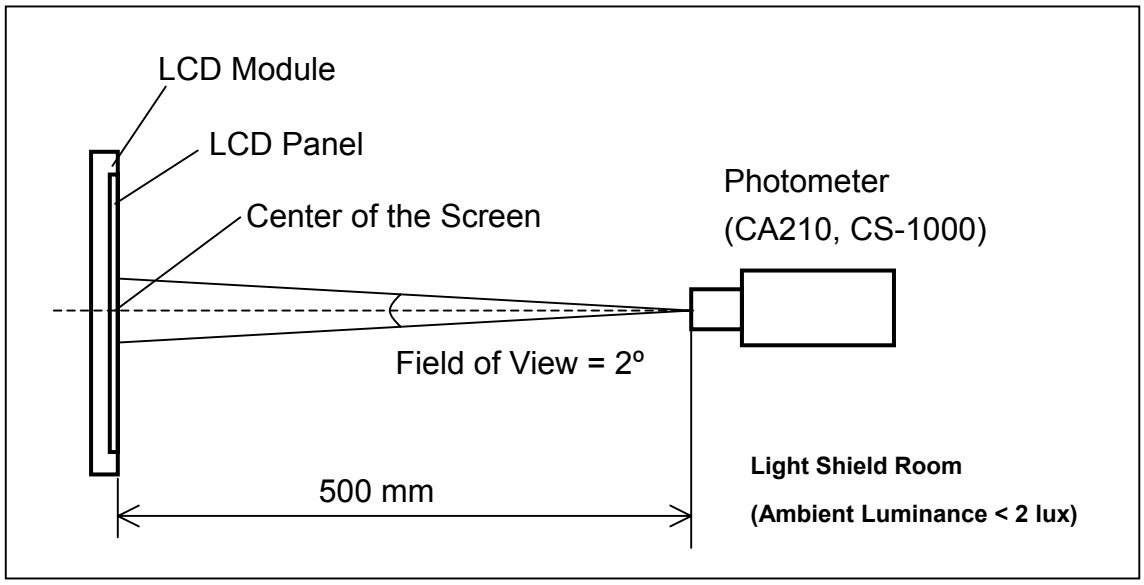
Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



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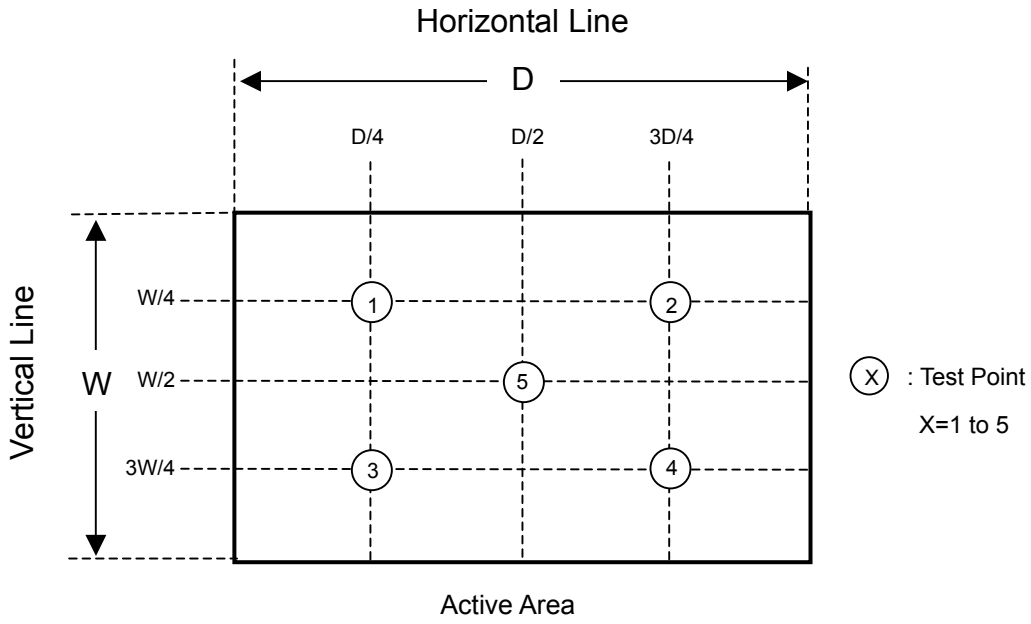
Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



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8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the lamp wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

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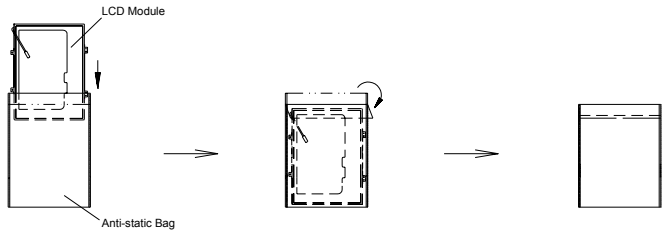
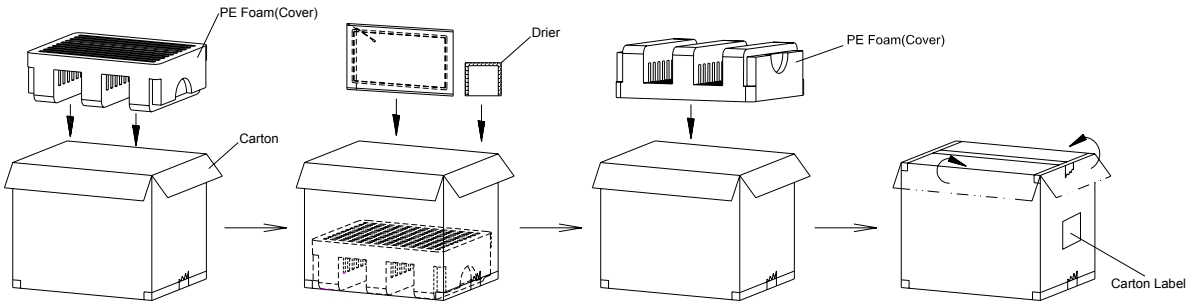
9. PACKING

9.1 CARTON



Box dimensions:422(L)x337(W)x345(H)mm
Weight:Appox. 7.5kg(10 module per 1 box)



Packing testing criteria :

(1) Packing drop : 1 corner, 3 edges, 6 faces, each direction for one time, follow ISTA standard.

(2) Packing vibration : Random, follow ISTA standard.

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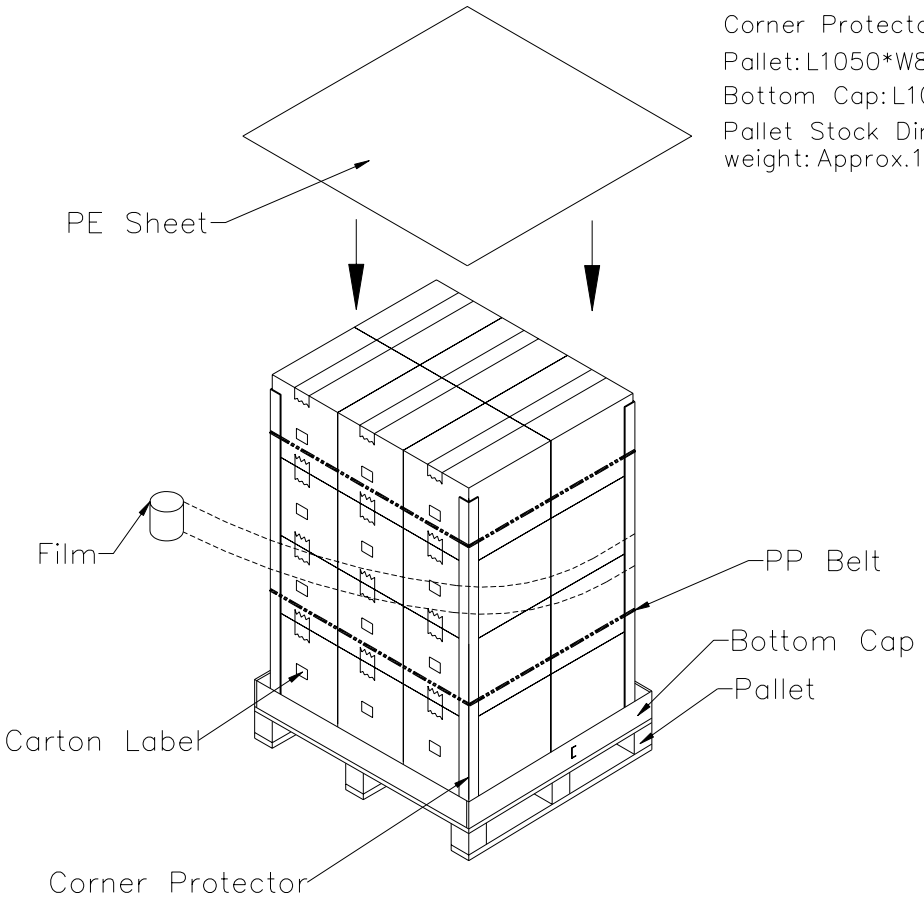
9.2 PALLET



Corner Protector: L1350mm*50mm*50mm
Pallet: L1050*W870*H135mm
Bottom Cap: L1050*W870*H120mm
Pallet Stock Dim: L1050*W870*H1380mm
weight: Approx.185kg

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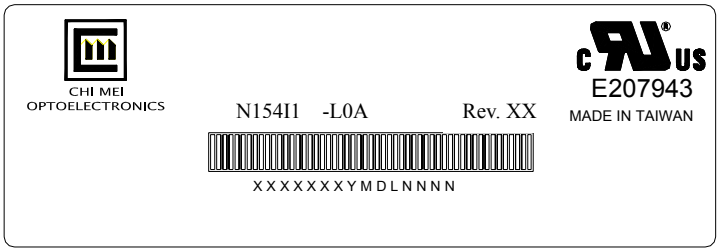
10. DEFINITION OF LABELS

10.1 CMO MODULE LABEL

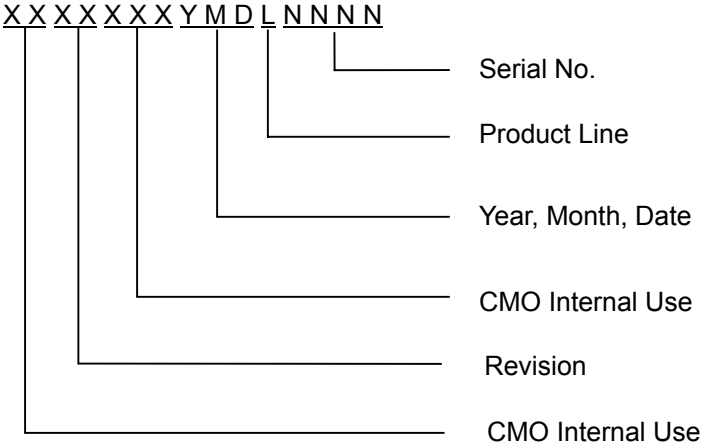
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: N154I1 - L0A

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

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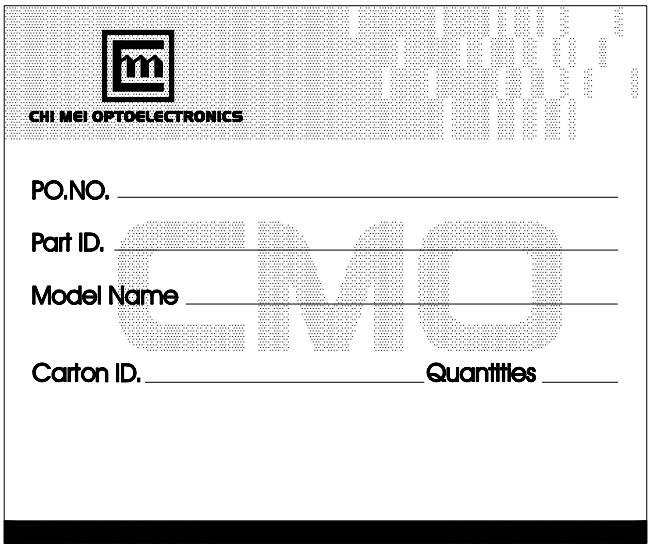
10.2 CARTON LABEL



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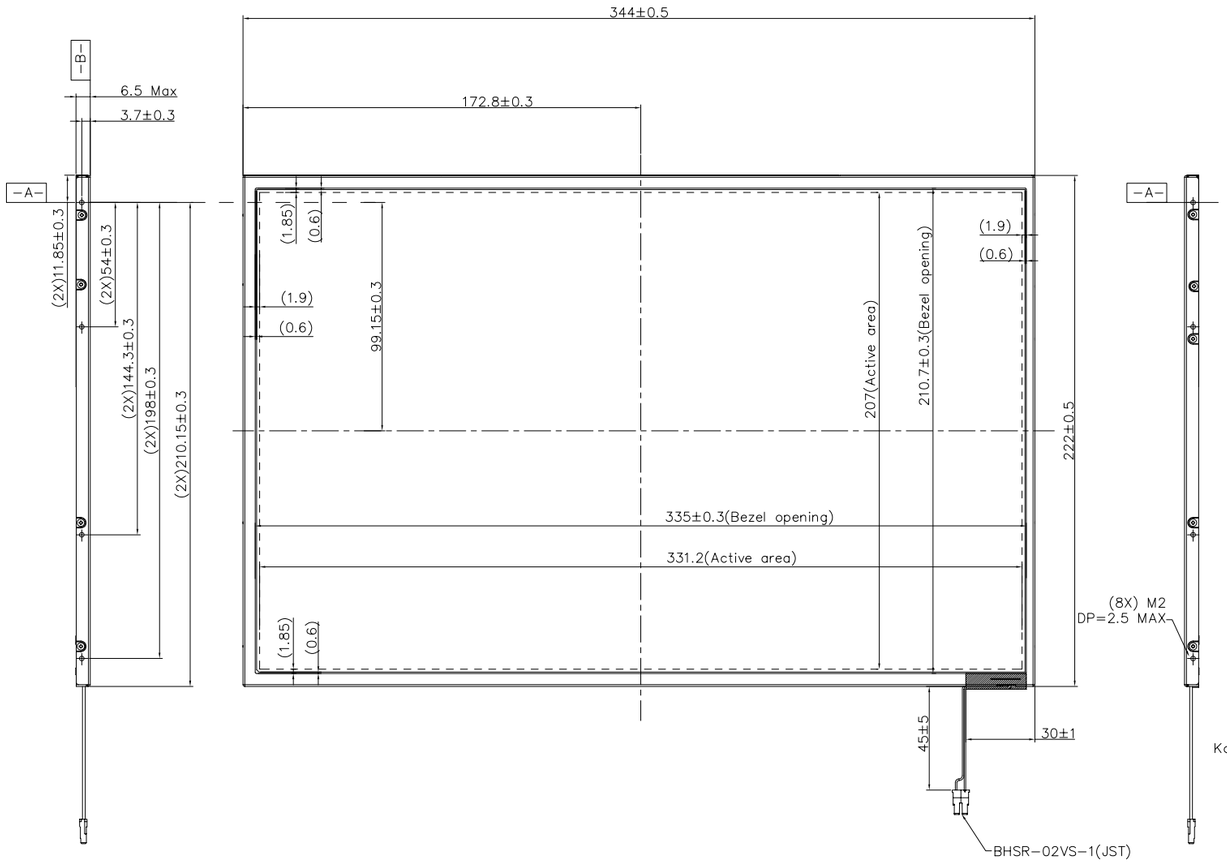
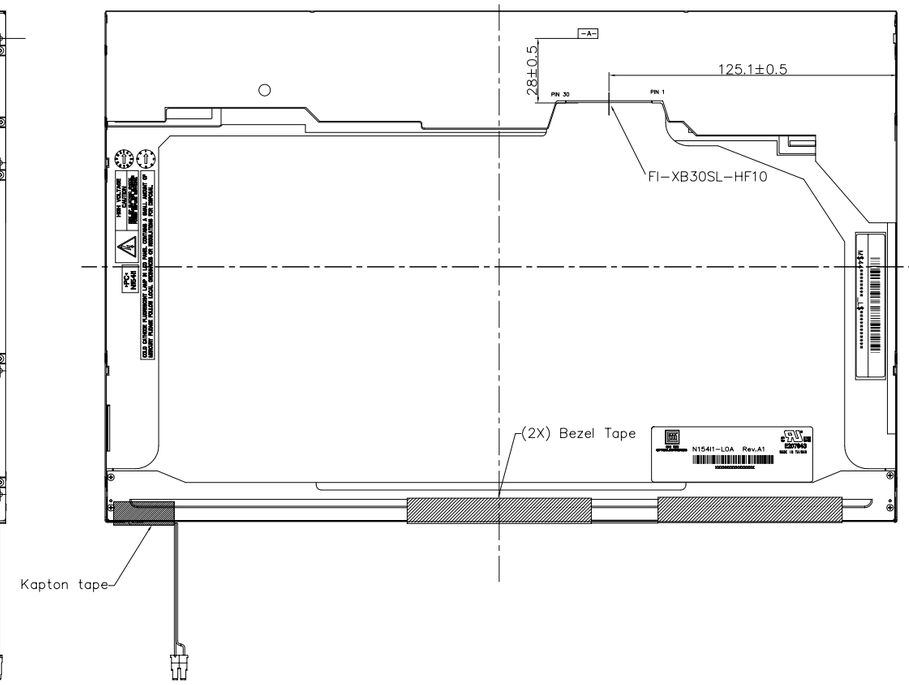
Notes:
1. General Tolerance : ±0.5
2. The screw torque for mounting shall not exceed 2.5kgf-cm.





Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

TITLE	Outline N154I1-L0A					2D REV.	1.0
						3D REV.	
Approved	Bill Sheu	Drawing No.	N154A41011				
Checked	Yule Lin	Part No.					
Drawer	Mulciber Hsieh	Material		Sheet	1 / 1	A3	
Designer	Mulciber Hsieh	Date	17-Jan-2004	Scale	1:1	Unit:mm	

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